PATENT

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July 3, 2002
Date

Ayesha S. Wilks

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Thomas W. Voshell	Attorney Docket No.:	500080.02
Serial No.	: 09/695,756	Group Art Unit	: 2133
Filed	: October 24, 2000	Examiner	: Guy J. Lamarre, P.E.
Title	: METHOD AND APPARATUS FOR REDUNDANT LOCATION ADDRESSING USING DATA COMPRESSION		

Box Non-Fee Amendment
Commissioner of Patents
Washington, DC 20231

RESPONSE TO OFFICE ACTION

Sir:

Claims 41-67 are pending in the present application. In the office action mailed May 17, 2002, the rejection of claims 41 and 45 under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 5,363,382 to Tsukakoshi ("the Tsukakoshi patent") have been maintained from the Office Action of January 16, 2002. The rejection of claims 42, 43, 46-48, and 54-64 under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent alone, or in view of U.S. Patent No. 5,881,221 to Hoang *et al.* ("the Hoang patent") was also maintained. Additionally, the indicated allowability of claims 44, 49-53, 65-67 set forth in the Office Action of January 16, 2002, has also been withdrawn in view of newly discovered prior art references.

Claims 44, 49-53, and 65-67 have also been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of U.S. Patent No. 4,642,793 to Meaden ("the Meaden patent"). Claims 44, 49-53, and 65-67 were further rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of U.S. Patent No. 5,659,737 to Matsuda ("the Matsuda patent"). Claims 44, 49-53, and 65-67 were still further rejected under

35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of IBM technical disclosure bulletin entitled, Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory, June 1, 1988 ("the IBM technical disclosure").

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the present invention are directed to a technique and system where memory locations in a spare memory array can be substituted for defective memory locations of a system memory. The addresses of the defective memory locations already determined to be defective are stored in a compressed format in a map memory array. Consequently, the number of memory cells needed to store a memory map of defective memory cells in the memory array can be smaller than if the address for each defective memory cell is stored for the memory map.

In operation, the addresses for the defective locations in the system memory are stored in a compressed format in a map memory array. A range of these compressed defective addresses are stored in an uncompressed format in a temporary memory array. When a requested memory address is presented to a storage control unit, a hash code for the requested memory address is compared to hash codes for the uncompressed defective address currently stored in the temporary memory array. In the event the hash code of the requested address matches one of the hash codes of the uncompressed defective addresses, then the address of the substitute memory location in a spare memory array corresponding to the matching hash code is provided by the temporary memory array to the storage control unit. The memory location in the spare memory corresponding to the address is then accessed.

In the event that the hash code does not match any of the hash codes for the uncompressed defective address currently stored in the temporary memory array, compressed defective address information in the range of the hash code of the requested address is found in the map memory, decompressed, and then stored in the temporary memory array. Then the hash code of the requested address is compared with the newly decompressed address. If there is a

hash code match, then the substitute address is provided by the temporary memory array to the storage control unit. If there is not a hash code match, the storage control unit assumes that the requested memory address is not a defective memory location, and proceeds to access the system memory using the requested address.

In contrast, the Tsukakoshi patent describes a method of memory fault analysis for redundancy memory repair using a fault analysis memory (FAM) that is smaller than the memory area of the memory under test (MUT). This is accomplished by taking advantage of the particular arrangement of redundancy memory of the MUT.

The Examiner has characterized the Tsukakoshi patent as teaching "when [sic] memory cell is determined as defective, means is provided for substitution of address of said memory cell with a different address of non-faulty memory cell." *Office Action* of May 17, 2002, page 2. However, this statement mischaracterizes the invention described in the Tsukakoshi patent. For example, the "comparison means" described in the Summary of the Invention refers to a *data* comparison means, which compares read data with the expected data to determine if a memory location is defective. *See* col. 2, lns. 18-23. Moreover, "address allocation" and "address compression" as described in the Tsukakoshi patent refer to allocation of a single memory location in the FAM to correspond to a plurality of memory cells of the MUT, which is not the address compression described in the specification of the present invention.

As described in the Summary of the Invention of the Tsukakoshi patent, the method described therein "performs address allocation for a fault analysis memory so that *plural number of memory cells* of a memory under test (MUT) correspond based on a predetermined rule to a *single memory cell* of a fault analysis memory." (Emphasis added) *See* col. 2, lns. 27-31. Unlike embodiments of the present invention, the method described in the Tsukakoshi patent does not store the address of defective memory locations in a compressed fashion, but merely stores a *flag* in a memory cell of the FAM which corresponds to multiple locations in the MUT, one of which is defective. Moreover, the invention of the Tsukakoshi patent does not compare a received address with any stored defective addresses, as in the claimed inventions, but rather compares *read data* and *expected data* generated by an algorithmic pattern generator. The location of the defective memory is never referenced in the method of the Tsukakoshi patent

because the invention is directed to storing defective memory locations during *testing* of the MUT.

The example described in the Tsukakoshi patent describes a MUT having a redundancy memory repair arrangement where redundant rows and columns of memory are replaced in pairs. That is, although only one row of memory cells may be defective, two rows of redundant memory are nevertheless substituted to repair the defective memory cells. Similarly, column redundancy are also substituted for defective memory cells in pairs. Thus, the method described in the Tsukakoshi patent takes advantage of this fact by having one memory location in the FAM correspond to four memory locations (arranged in a 2-by-2 square) in the MUT. That is, if *any* of the four memory cells are defective, then the corresponding single memory location in the FAM stores a flag indicating that at least one of four cells in the MUT are defective and need to be replaced by redundancy memory.

Where the number of redundant memory rows are columns substituted for defective memory locations in the MUT are greater than two, the "compression" ratio of the method described by the Tsukakoshi patent would be increased. For example, if four redundant rows and columns are used when a replacement is made, then one memory location in the FAM could correspond to sixteen memory locations (arranged in a 4-by-4 square) in the MUT. Consequently, where any one of those sixteen memory cells of the MUT are defective, the single memory location in the FAM corresponding to those sixteen cells will store a flag indicating a defective memory that needs to be replaced by redundancy.

Claims 41 and 45 are clearly patentably distinct from the teachings of the Tsukakoshi patent. It is well established that in order for an Examiner to establish a *prima facie* case of anticipation, the Examiner must be able to show that a reference teaches every element of a claim. *See* MPEP, section 2131. As previously discussed, the Examiner has failed to establish a *prima facie* case of anticipation based on the Tsukakoshi patent because the Examiner has not shown where or how the Tsukakoshi patent teaches the combination of elements recited in claims 41 and 45.

Claim 41 recites a method for accessing a memory, comprising comparing *a memory address* of a memory access request to *defective memory addresses* stored in a compressed format, the defective memory addresses having substitute addresses associated and

stored therewith, where the memory address matches one of the stored defective memory addresses, extracting the substitute address associated therewith, and accessing a memory location corresponding to the extracted substitute address rather than a memory location corresponding to the memory address. Despite the Examiner's characterization of what the Tsukakoshi patent teaches, the claimed invention of claim 41 is not anticipated. The Tsukakoshi patent does not teach, among other things, comparing a memory address, extracting a substitute address, or accessing a memory location corresponding to the extracted substitute address. As previously discussed, the Tsukakoshi patent merely describes using a single memory location of a FAM to represent multiple memory locations in a MUT. The number of MUT memory locations one FAM memory cell represents depends on the number of redundant memory cells that are necessarily replaced when even one MUT memory cell is found to be defective.

Claim 45 recites a method for accessing a memory device receiving memory addresses, the method comprising comparing the received memory addresses to addresses of defective memory locations in the memory device, the addresses of the defective memory locations having associated therewith substitute addresses corresponding to substitute memory locations in another memory, and substituting for the memory addresses matching the addresses of defective memory locations the associated substitute memory addresses to access the substitute memory locations in the other memory. As with claim 41, the examiner has failed to show how the Tsukakoshi patent describes the combination of elements recited in claim 45. For example, the Tsukakoshi patent does not describe comparing a received memory address to addresses of defective memory locations or substituting for the memory addresses matching the addresses of defective memory locations the associated substitute memory addresses to access the substitute memory locations in the other memory.

For the foregoing reasons, the rejection of claims 41 and 45 under 35 U.S.C. 102(a) as being anticipated by the Tsukakoshi patent cannot be maintained. Therefore, the rejection of claims 41 and 45 should be withdrawn.

With respect to the rejection of claims 42, 43, 46-48, and 54-64 under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent, alone and in combination with the Hoang patent, the Examiner has also failed to establish a *prima facie* case of obviousness. It is

also well known that in order to establish a prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *See* MPEP, section 2143.03.

The Examiner has stated that the Tsukakoshi patent fails to specifically show the decompressing of addresses for comparison. According to the Examiner, "it would have been obvious to a person having ordinary skill in the art at the time the invention was made to decompress address for comparison." *Office Action* of January 16, 2002, page 3. Moreover, the Examiner has stated that Tsukakoshi does not specifically teach temporary storage of defective memory cell addresses during power-up, however, the Hoang patent teaches power-on self testing of a computer system including a memory cell. *Id.*

The problem, however, is that the Tsukakoshi patent fails to describe the claimed in invention to such a great degree that the knowledge stated by the Examiner as being obvious, and the teachings of the Hoang patent as characterized by the Examiner, cannot make up for the deficiencies of the Tsukakoshi patent. For example, as previously discussed, the Tsukakoshi patent does not describe any of the limitations of comparing addresses, extracting a substitute address, or accessing a memory location corresponding to the extracted substitute address. Even if we assume that it would have been obvious to one in the art to decompress addresses for comparison, the Tsukakoshi patent never describes comparing addresses in the first place or determining whether a memory address matches an address of a defective memory cell. Similarly, if we assume that the Hoang patent does teach testing upon power-up, combining that teaching with the teachings of the Tsukakoshi patent fail to suggest the combination of limitations of the recited claims. What does it matter if testing is performed upon power up when the memory addresses are never stored, and received address or hash codes generated from received address are never compared with stored addresses or hash codes of defective memory locations? Clearly, any combination of references based on the Tsukakoshi patent will fail to render the claims of the present application unpatentable.

For the foregoing reasons, claims 42, 43, 46-48, and 54-64 are patentable over the Tsukakoshi patent, alone or in combination with the Hoang patent or the subject matter found to be obvious by the Examiner. Therefore, the rejection of claims 42, 43, 46-48, and 54-64 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, claims 44, 49-53, and 65-67 have been newly rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of the Meaden patent. As stated by the Examiner, the Tsukakoshi patent fails to disclose "the step whereby calculating a value from the memory address comprises dividing the value represented by the memory address by a prime number or use of hashing code or function." *Office Action* of May 17, 2002, page 3. The Examiner cites the Meaden patent as teaching the technique of address generation not done so by the Tsukakoshi patent, and states that it would have been obvious to modify the teachings of the Tsukakoshi patent by the teachings of the Meaden patent.

Claims 44, 49-53, and 65-67 were further rejected under 35 U.S.C. 103(a) as being unpatentable over the Tsukakoshi patent in view of the Matsuda patent, and also as being unpatentable over the Tsukakoshi patent in view of the IBM technical disclosure. In both cases, the secondary reference was cited to essentially teach "calculating a value from the memory address compris[ing] dividing the value represented by the memory address by a prime number or use of hashing code or function." *Id.* at pages 4 and 5.

As previously discussed, the Tsukakoshi patent fails to teach the limitations of the rejected claims as described by the Examiner. Consequently, the secondary references which teach the use of prime numbers or hashing code functions does not make up for the deficiencies of the Tsukakoshi patent. Namely, claim 49 recites a method for accessing a requested memory location of a memory array, the requested memory location having a requested address, the method comprising generating a first hash code from the requested address, comparing the first hash code to hash codes for decompressed addresses stored in a temporary memory array, when a match is found between a hash code for a decompressed address and the first hash code, determining if an address stored in the temporary array corresponds to the requested address, and accessing a spare memory array when an address stored in the temporary array corresponds to the requested address.

The Tsukakoshi patent fails to describe several limitations in addition to the use of hash codes, which according to the Examiner, are taught by the Meaden patent, the Matsuda patent, or the IBM Technical disclosure. For example, the Tsukakoshi patent does not describe comparing hash codes of the requested address with the hash codes of the decompressed addresses, determining if any address stored in the temporary array correspond to the requested

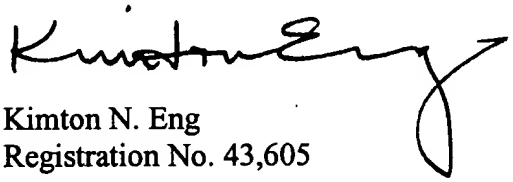
address, or accessing a spare memory array when an address stored therein corresponds to the requested address. As previously discussed, the method described in the Tsukakoshi patent does not include storing addresses, does not make address comparisons, and does not access spare memory array. All the Tsukakoshi patent describes is storing a error flag bit in a memory location of a FAM that corresponds to multiple memory locations of a MUT. The number of multiple memory locations represented by each memory location of the FAM is dictated by the specific redundancy arrangement of the MUT. The method of the Tsukakoshi patent does not involve any address comparison because no addresses are stored, and more significantly, the method of the Tsukakoshi patent is directed to logging defective memory locations, not substitution of good memory for defective memory locations.

Consequently, claim 49 is patentable over the Tsukakoshi patent in view of the Meaden patent, the Matsuda patent, or the IBM technical disclosure. Therefore, the rejection of claim 49 under 35 U.S.C. 103(a) should be withdrawn. Similarly, claim 44, which depends from claim 41, claims 50-53, which depend from claim 49, and claims 65-67, which depend from claim 64, are also allowable because of their dependency from respective allowable base claims. Each of the dependent claims further narrow the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. However, because each claim in an application represents a different invention, the rejection of an independent claim does not necessarily result in the rejection of claims depending therefrom. For the foregoing reasons, the rejection of claims 44, 50-53, and 65-67 under 35 U.S.C. 103(a) should also be withdrawn.

All of the claims remaining in the application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is requested to contact the undersigned at the number listed below for a telephone interview if, upon consideration of this amendment, the Examiner determines any pending claims are not in condition for allowance. The undersigned also requests the Examiner to direct all future correspondence to the address set forth below in the event the Examiner shows a different correspondence address for the attorney of record.

Respectfully submitted,

DORSEY & WHITNEY LLP



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